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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/788,805	02/27/2004	Reidar Lindstedt	2002 P 16328 US	7850

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EXAMINER	
VU, HUNG K	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 09/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/788,805	LINDSTEDT, REIDAR	
	Examiner	Art Unit	
	Hung Vu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 July 2005*.

2a)☐ This action is FINAL. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) *14-19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *06/21/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election of Invention of Group I, Claims 1-13, in the reply filed on 07/22/05 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Applicant's election without traverse of Invention of Group I, Claims 1-13 in the reply filed on 07/22/05 is acknowledged.

Claims 14-19 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected Invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 07/22/05.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Glen (PN 6,518,659).

Glen discloses, as shown in Figures 2-6D, a semiconductor chip arrangement comprising:

a mount element (31);

a first semiconductor substrate (10,44) including at least one interconnect (21) formed on the first semiconductor substrate and also including at least one contact area (26) that is electrically connected to the interconnect and is arranged on a side surface of the first semiconductor substrate; and

a second semiconductor substrate (10,44) having at least one interconnect (21) formed on the second semiconductor substrate and also including at least one contact area (26) that is electrically connected to the interconnect and is arranged on a side surface of the second semiconductor substrate;

wherein the second semiconductor substrate is arranged on the first semiconductor substrate and the first semiconductor substrate is arranged on the mount element such that a first main surface of the second semiconductor substrate rests on the first semiconductor substrate, and a first main surface of the first semiconductor substrate rests on the mount element, and wherein an electrical contact is produced between the contact area on the first semiconductor substrate and the contact area on the second semiconductor substrate.

Regarding claim 2, Glen discloses the first and second semiconductor substrates each have an integrated circuit disposed in the area of the first main surface, wherein the integrated circuit is electrically coupled to the interconnect.

Regarding claim 3, Glen discloses the semiconductor chip arrangement further comprising a conductive material (portion of 21, 26) applied between the contact area on the first semiconductor substrate and the contact area on the second semiconductor substrate.

Regarding claim 4, Glen discloses the first main surface of the first semiconductor substrate is attached to the mount element.

Regarding claim 5, Glen discloses the contact area on the first semiconductor substrate and the contact area on the second semiconductor substrate each extend from the first main surface to a second main surface of the respective semiconductor substrate.

Regarding claim 6, Glen discloses each of the first and second semiconductor substrates includes a dynamic random access memory formed therein.

Regarding claim 7, Glen discloses, as shown in Figures 2-6D, a semiconductor chip arrangement comprising:

a mount element (not shown, 31);

a first semiconductor substrate (44) arranged over the mount element, the first semiconductor substrate including at least one interconnect (upper of 21) formed thereon, the first semiconductor substrate further including at least one contact area (side of 21) that is electrically connected to the interconnect and is arranged along a side surface of the first semiconductor substrate;

a second semiconductor substrate (44) arranged over the mount element alongside the first semiconductor substrate, the second semiconductor substrate including at least one interconnect (upper of 21) formed thereon, the second semiconductor substrate further including

at least one contact area (side of 21) that is electrically connected to the interconnect and is arranged along a side surface of the second semiconductor substrate, the second semiconductor substrate arranged so that an electrical contact is produced between the contact area of the first semiconductor substrate and the contact area of the second semiconductor substrate; and

a third semiconductor substrate (44) arranged over the second semiconductor substrate, the third semiconductor substrate including at least one interconnect (upper of 21) formed thereon, the third semiconductor substrate further including at least one contact area (side of 21) that is electrically connected to the interconnect and is arranged along a side surface of the third semiconductor substrate, the third semiconductor substrate arranged so that an electrical contact is produced between the contact area of the third semiconductor substrate and the contact area of the second semiconductor substrate.

Regarding claim 8, Glen discloses the first, second and third semiconductor substrates each have an integrated circuit (28) disposed therein, wherein the integrated circuit is electrically coupled to the interconnect.

Regarding claim 9, Glen discloses the semiconductor chip arrangement further comprising a conductive material (portion of 21) applied between the contact area on the first semiconductor substrate and the contact area on the second semiconductor substrate.

Regarding claim 10, Glen discloses the first semiconductor substrate is attached to the mount element and wherein the second semiconductor substrate is attached to the mount element.

Regarding claim 11, Glen discloses the contact areas on the first and the second semiconductor substrates each extend from a first main surface to a second main surface of the respective semiconductor substrate.

Regarding claim 12, Glen discloses the contact area on the third semiconductor substrate extends to a first main surface on the third semiconductor substrate.

Regarding claim 13, Glen discloses each of the first, second, and third semiconductor substrates includes a dynamic random access memory formed therein.

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hung K. Vu whose telephone number is (571) 272-1666. The examiner can normally be reached on Tuesday-Friday 6:00-4:30, Eastern Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's acting supervisor, Steven Loke can be reached on (571) 272-1657. The Central Fax Number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Vu

September 2, 2005

Hung Vu

Primary Examiner